

U.S. Patent Application No. 10/805,006
Attorney Docket No. 352161-991140 (Formerly 2102651-991140)

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) An integrated circuit device including clock routing, comprising:
 - a first node;
 - a plurality of wires branching from the first node;
 - a second node which first appears on a first wire of the plurality of wires; and
 - a wire connecting only to a third node which exists in a direction within angles of 90 degrees from an input direction of a signal inputted to the second node.
2. (Original) An integrated circuit device including clock routing, comprising:
 - a first node;
 - a plurality of wires branching from the first node;
 - a second node which first appears on a first wire of the plurality of wires; and
 - a wire connecting only to a third node which exists in a direction within angles of 45 degrees from an input direction of a signal inputted to the second node.
3. (Original) An integrated circuit device including clock routing for setting of a target delay, comprising:
 - a node;
 - a next-stage node to which a signal is to be sent after the node; and
 - a combination of any of wires in directions at angles of less than 90 degrees from a straight direction connecting the node with the next-stage node.
4. (Original) An integrated circuit device including clock routing for setting of a target delay, comprising:
 - a node;
 - a next-stage node to which a signal is to be sent after the node; and
 - at least one wire in a wiring direction present in a quadrant of a straight direction connecting the node with the next-stage node.

U.S. Patent Application No. 10/805,006
Attorney Docket No. 352161-991140 (Formerly 2102651-991140)

5. (Withdrawn) A clock layout system, comprising:
a clock routing processing unit placing a route driver on a semiconductor chip and performing clock routing with an H-tree structure in a local area and with a star structure in a global area based on circuit information on a logic circuit;
a second node specifying unit specifying, as a second node, a node that first appears on a first wire among a plurality of wires branching from an arbitrary first node in the logic circuit;
a third node specifying unit specifying, as a third node, at least one node that is the second to appear on a wire other than the first wire among the plurality of wires branching from the first node;
a third node defining unit defining, as the defined third node, only the third node that exists in a direction within a predetermined angle from an input direction of a signal inputted to the second node, among the third nodes; and
a folding executing unit folding a wire from the first node up to the defined third node and a node present therebetween.
6. (Withdrawn) The clock layout system according to claim 5, wherein the predetermined angle used by the third node defining unit is 90 degrees.
7. (Withdrawn) The clock layout system according to claim 5, wherein the predetermined angle used by the third node defining unit is 45 degrees.
8. (Withdrawn) A clock layout system, comprising:
a wiring direction determining unit determining at least one wiring direction used for connecting an arbitrary node in a logic circuit with a next-stage node to which a signal is to be sent after the node; and
a wire ratio calculating unit calculating a wire ratio of the wiring direction so that a capacitance moment or delay time becomes equal to another one.
9. (Withdrawn) The clock layout system according to claim 8, wherein the wiring direction determining unit determines, as the wiring direction, a combination of any of wiring directions at

U.S. Patent Application No. 10/805,006
Attorney Docket No. 352161-991140 (Formerly 2102651-991140)

angles

of less than 90 degrees from a straight direction connecting
the node with the next-stage node.

10. (Withdrawn) The clock layout system according to claim 8, wherein the wiring direction determining unit determines, as the wiring direction, a combination of any of wiring directions present in a quadrant of a straight direction connecting the node with the next-stage node.

11. (Withdrawn) A clock layout method, comprising:
accepting circuit information on a logic circuit;
based on the circuit information, placing a route driver on a semiconductor chip and
forming initial clock routing with an H-tree structure in a local area and with a star structure in a global area;

specifying, as a second node, a node which first appears on a first wire among a plurality of wires branching from an arbitrary first node in the initial clock routing;

specifying, as a third node, at least one node which is the second to appear on a wire other than the first wire among the plurality of wires branching from the first node;

defining, as the defined third node, only the third node which exists in a direction within a predetermined angle from an input direction of a signal inputted to the second node, among the third nodes; and

folding a wire from the first node up to the defined third node and a node present therebetween.

12. (Withdrawn) The clock layout method according to claim 11, wherein the predetermined angle is 90 degrees.

13. (Withdrawn) The clock layout method according to claim 11, wherein the predetermined angle is 45 degrees.

14. (Withdrawn) A clock layout method, comprising:
accepting circuit information on a logic circuit;

U.S. Patent Application No. 10/805,006
Attorney Docket No. 352161-991140 (Formerly 2102651-991140)

determining at least one wiring direction used for connecting an arbitrary node in the logic circuit with a next-stage node to which a signal is to be sent after the node; and

calculating a wire ratio of the wiring direction so that a capacitance moment or delay time becomes equal to another one.

15. (Withdrawn) The clock layout method according to claim 14, wherein the step of determining the wiring direction is a step of determining, as the wiring direction, a combination of any of wiring directions at angles of less than 90 degrees from a straight direction connecting the node with the next-stage node.

16. (Withdrawn) The clock layout method according to claim 14, wherein the step of determining the wiring direction is a step of determining, as the wiring direction, a combination of any of wiring directions present in a quadrant of a straight direction connecting the node with the next-stage node.

17. (Withdrawn) A clock layout program causing a computer to execute:
accepting circuit information on a logic circuit;
based on the circuit information, placing a route driver on a semiconductor chip and forming initial clock routing with an H-tree structure in a local area and with a star structure in a global area;

specifying, as a second node, a node which first appears on a first wire among a plurality of wires branching from an arbitrary first node in the initial clock routing;

specifying, as a third node, at least one node which is the second to appear on a wire other than the first wire among the plurality of wires branching from the first node;

defining, as the defined third node, only the third node which exists in a direction within a predetermined angle from an input direction of a signal inputted to the second node, among the third nodes; and

folding a wire from the first node up to the defined third node and a node present therebetween.

18. (Withdrawn) A clock layout program causing a computer to execute: accepting circuit

U.S. Patent Application No. 10/805,006
Attorney Docket No. 352161-991140 (Formerly 2102651-991140)

information on a logic circuit; determining at least one wiring direction used for
connecting an arbitrary node in the logic circuit with a next-stage node to which a signal
is to be sent after the node; and
calculating a wire ratio of the wiring direction so that a capacitance moment or delay time
becomes equal to another one.